



# تلخيص لغة تجميع ومعالجات دقيقة

إرادة - ثقة - تغيير

Parallel processing → That we have Two units ~~works~~ works at the same time to increase speed of processing CH 2

First one bus interface unit that fetch instruction from memory & store it in place close to microprocess.

second one ~~inter~~ execution unit that execute the instruction

data bus → carry data info  
address bus → carry address info

→ Components in BIU

- 1) Segment Register → base address
- 2) Instruction pointer (IP) → offset address
- 3) Address generation adder → Convert logical to physical address  
32 bits → 20 bits
- 4) Bus control logic.
- 5) instruction queue → place to store ~~inst~~ instruction

→ Components in EU

- 1) ALU
- 2) status & control flag
- 3) general-purpose Registers
- 4) Temporary-operand Registers

\* we have 14 Register inside Microprocessor each one's size 16-bits

1) Four segment Registers → base address

CS, DS, ES, SS → base address

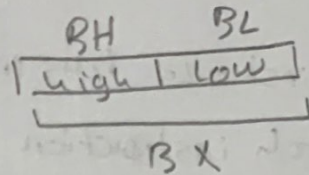
CS → base address Code Segment  
DS → base address data segment  
ES → base address Extra segment  
SS → stack segment

store code or instruction  
store data that need to be process  
store status info

1] ~~Inst~~ instruction pointer (IP) → offset address

2] Four data Registers

AX, BX, DX, CX  
 Accumulator Base Data Count

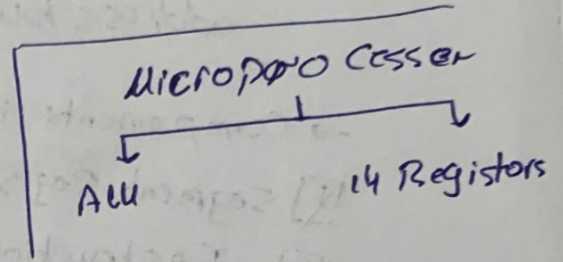


↓  
 offset address for data seg / Extra

3] Two pointer Registers → offset address for stack segment

BP, SP → Top of the stack

any location within the stack

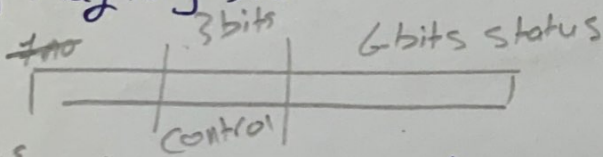


4] Two index Registers

SI, DI

↓  
 offset address for data & Extra segments

5] Flag Register



→ memory → 16 locations each one store 8 bits have  
 contain 4-segments each one store 64 h location  
 base (CS) # of address-bit = 2

1] Code segment  
 ↳ to store code & instructions  
 ↳ offset (IP)

2] Data segment  
 ↳ base (DS) # of address-bit = log # of bits = 100  
 ↳ offset (SI, DI, BX)

3] Extra segment  
 ↳ to store the data that need to be process  
 ↳ base (ES)  
 ↳ offset (SI, DI, BX)

4] Stack segment  
 ↳ to store status info  
 ↳ base (SS)  
 ↳ offset (BP, SP)

→ Even OR odd addressed Word

Aligned word even address

↳ LSB (0, 2, 4 & 6 --)  
(for the address)

mis Aligned word odd address

↳ LSB (1, 3, 5 --)  
(for the address)

→ double Word ( 32 bits = 4 bytes)

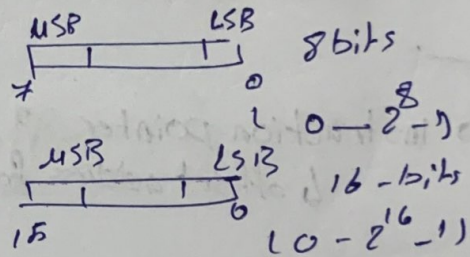
↳ address multiples of 4 → Aligned

↳ address not multiples of 4 → mis Aligned

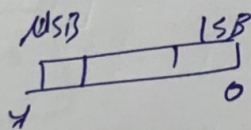
→ data Types

Integer } signed OR unsigned  
          } Byte-wide OR word-wide integer

\* ~~signed~~ unsigned

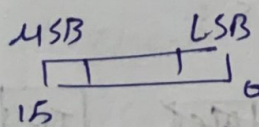


\* signed  
MSB } 0 → +ve  
      } 1 → -ve



8 bits ( -2<sup>7</sup> - 2<sup>8</sup>-1 )

\* signed  
MSB } 0 → +ve  
      } 1 → -ve



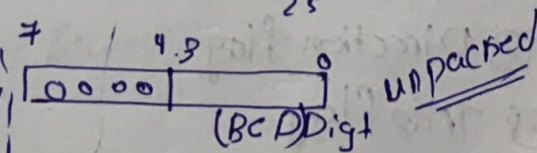
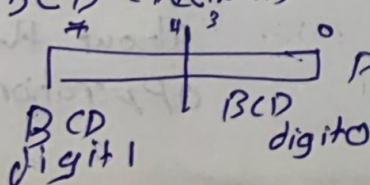
16 bits ( -2<sup>15</sup> - 2<sup>16</sup>-1 )

-ve number → 2<sup>i</sup> complement

1) toggle

2) 10011-1

1) BCD (Decimal)

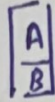


B) symbol

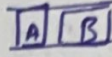
(ASCII) → وبتو ف ٨٠٠ Hex si Dec وبتو ف ٨٠٠  
دبتو ف ٨٠٠  
↓  
↓

→ memory segmentation.

1) Contiguous



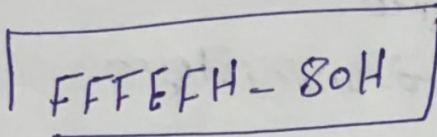
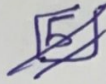
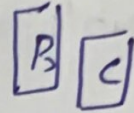
2) adjacent



3) disadjacent



4) over lapping



→ ف٨٠٠، ف٨٠٠، ف٨٠٠، ف٨٠٠  
memory

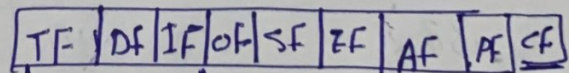
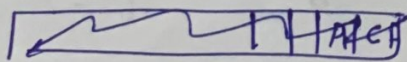
→ instruction pointer → point to the next instruction to fetch  
↳ offset address for CS

0000H → FFFFH

→ instruction execution queue

max size → 8088 → 4  
↳ 8086 → 6

→ status & control flags.



control flags

control flags

status flags

1) Interrupt flag

2) Direction flag

3) Trap flag

gives condition about the last operation

4)

→ status flags

1) carry flag (CF)  $\left\{ \begin{array}{l} 1 \text{ bit's carry value is 1} \\ 0 \text{ bit's carry value is 0} \end{array} \right.$

2) zero flag (ZF)  $\left\{ \begin{array}{l} 1 \text{ Zero = Result is zero} \\ 0 \text{ Result \neq zero} \end{array} \right.$

3) sign flag SF USB  $\left\{ \begin{array}{l} 1 \text{ USB = -1} \\ 0 \text{ USB = 0} \end{array} \right.$

4) overflow flag OF  $\left\{ \begin{array}{l} 1 \text{ carry in } \neq \text{ carry out} \\ 0 \text{ carry in = carry out} \end{array} \right.$

5) parity flag PF  $\left\{ \begin{array}{l} 1 \rightarrow \# \text{ of ones even} \\ 0 \rightarrow \# \text{ of ones odd} \end{array} \right.$   
 # of ones in 2 bits is 2

6) Auxiliary flag AF  $\left\{ \begin{array}{l} 1 \text{ 2 bits is parity/carry value is 1} \\ 0 \text{ 2 bits is parity/carry value is 0} \end{array} \right.$

physical address =  $\left[ \begin{array}{l} \text{shifted} \\ \text{Base} \\ (\text{Base 0}) \end{array} + \text{offset address} \right] \rightarrow 20 \text{ bits}$

logical address is 32 bits

aliases address

More than one logical address have the same physical in the same segment

→ stack segment

\* differences between stack segment & others

1) deal with word data only

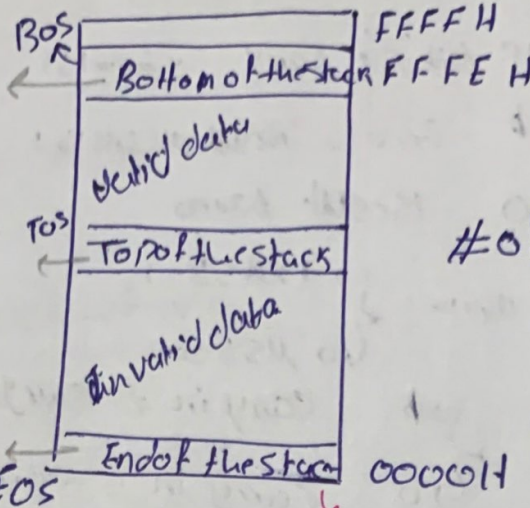
2) starting store data from lowest to highest

→ 1101 Instruction

Stack

→

Highest address word



Size = 4K byte

↳ 32 word

↓  
ابتداء

Last data location in which data has pushed

# of Invalid words

$$= \frac{TOS - EOS}{2}$$

Lowest address word

\* تعداد کلمات با آدرس نامعتبر

address 5B

POP → inc<sup>2</sup> by 2 bytes

↓  
مقدار

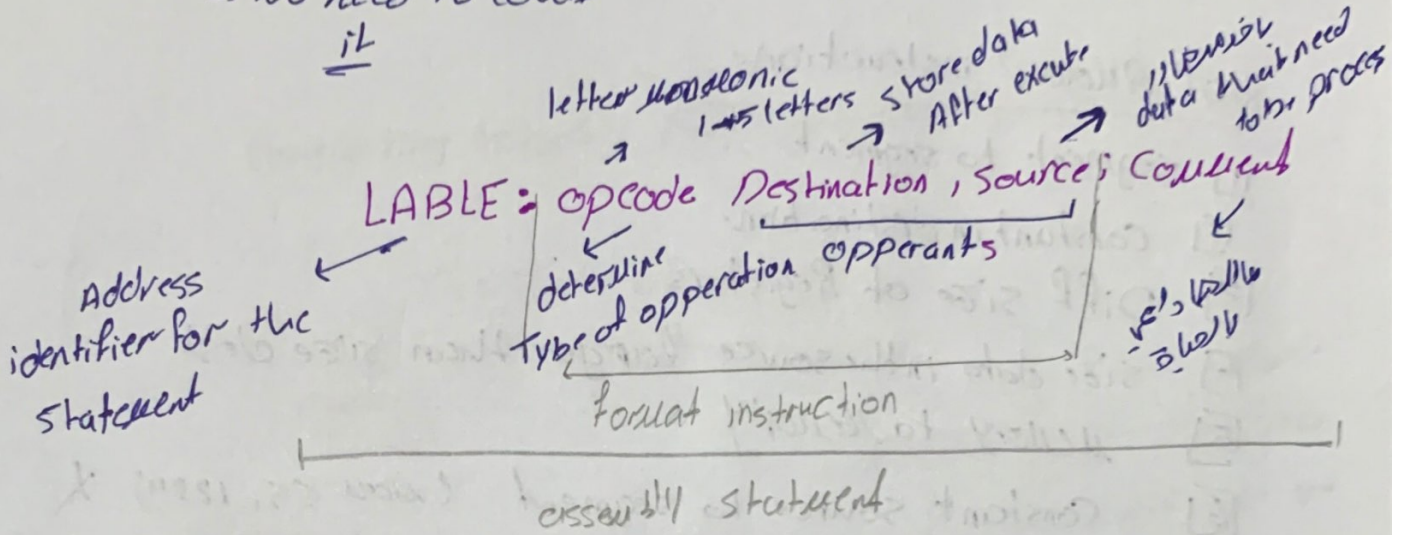
push → dec address 5B by 2 bytes

# Instructions

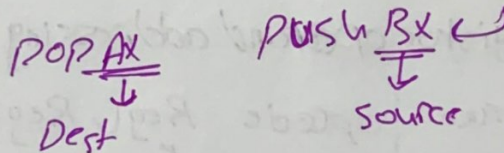
directive  
(Assembler)  
↳ convert assembly  
to machine code

executable  
(Microprocessor)  
it's need to convert  
from Assembly to machine  
code

↳ No need to convert  
it



opcode) source si Dest → one operand



assembler ( ~~not~~ assembly code → machine code )

compiler ( any language → machine code )

low level language → use physical component in the processor  
 high level language → use general variables that's closer to human

\* Both of them must be convert to machine code

\* low level language faster than other one



## → MOV Instruction

Meaning	Meaning	Format	Operation	Flags
MOV	Move	MOV DS	(S) → (D)	<u>None</u>

Ex: ~~MOV~~ Dest ← Source // i.e. data // copy

### NOT Allowed instructions

- 1] segment to segment
- 2] constant in destination.
- 3] Diff size of Registers
- 4] size data in the source larger than size dest
- 5] memory to memory
- 6] constant source to segment (MOV CS, 1234) ✗

### \* Addressing modes

#### 1] Register operand addressing mode

both Dest & source are Registers | opcode Reg1, Reg2 | MOV BX, AX  
Dest → Source

#### 2] Immediate operand addressing mode

Data is constant in source & Dest is Reg | opcode Reg, ImmX | MOV AL, 15H

#### 3] Memory addressing modes

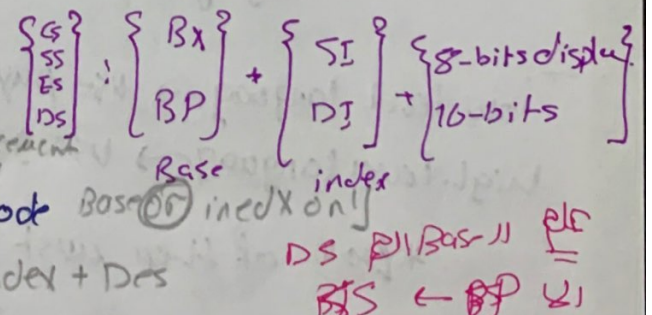
↳ Direct addressing mode

↳ Register indirect addressing mode

↳ Indexed addressing mode

↳ Based addressing mode

↳ Based-Indexed addressing mode



➔ Advantage of hybrid length

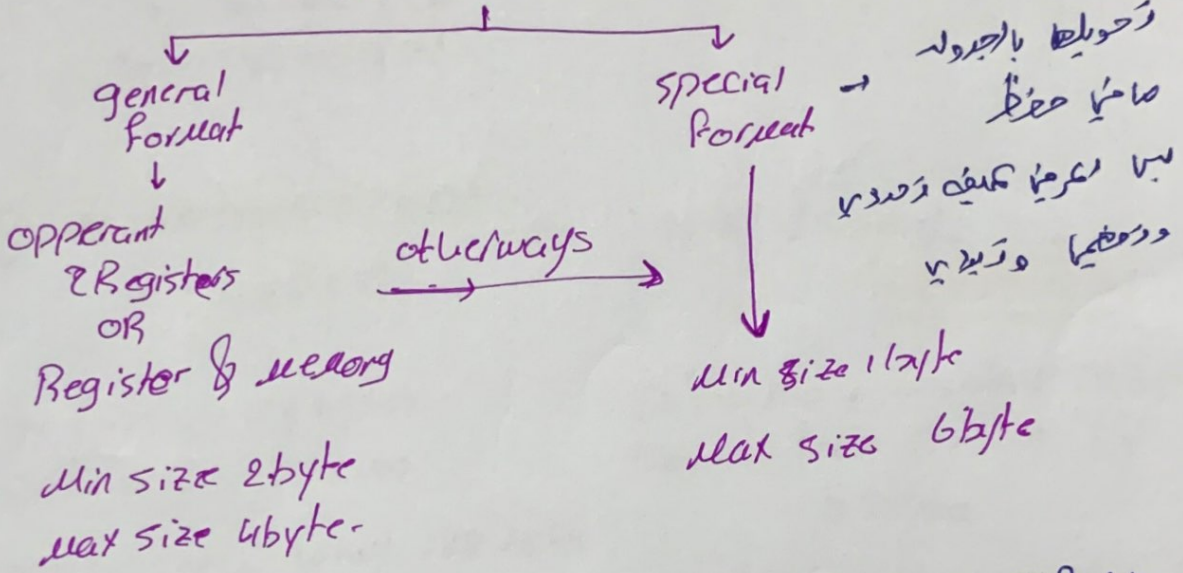
- 1) allows for many addressing modes
- 2) allows full size (32-bit) immediate data & addresses

➔ Disadvantage of Variable length

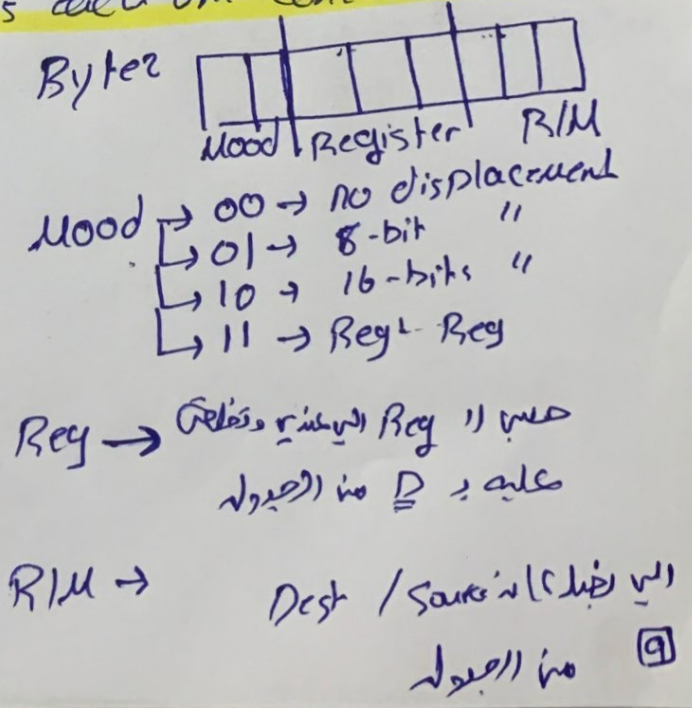
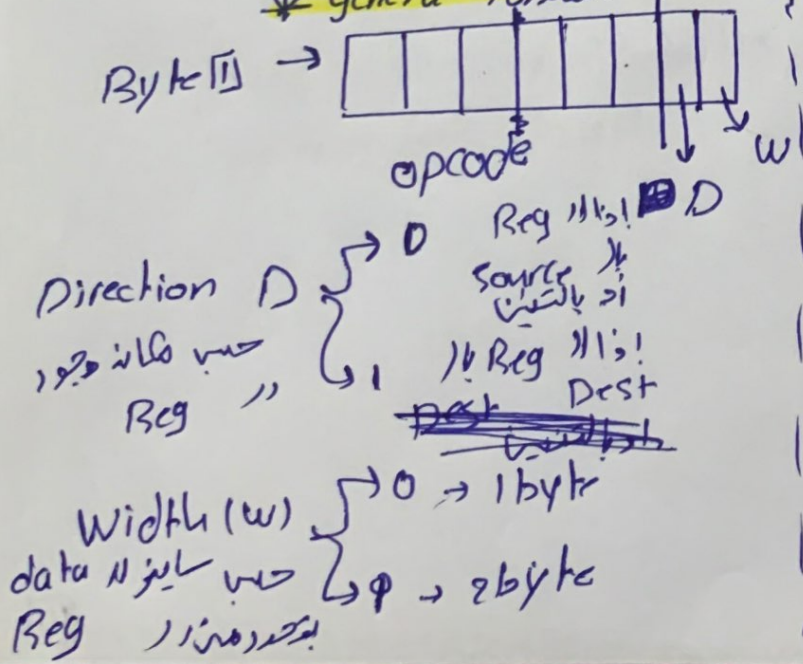
& need more complex assembler

converting assembly language instruction to Machine Code

Two Type of instructions



\* general format → 2 bytes each one contain 3 fields



# → DEBUG Program.

↳ An initial state when with the loading of DEBUG

IP → 0100

Status Register → 0040 (Interrupt flag = 1)  
Flag

1] Register Command (R) ⇒ Display & modify instructions  
R [Register Name]

R AX  
AX رجیٹر  
رجیٹر کے نام

R ( )  
رجیٹر کے نام  
Flags + Registers + Machine Code

2] Dump Command (D) ⇒ Display / Show  
D [ADDRESS] Default DS

D → Display 128 bytes  
starting from DS:0100

D 1373:200 → Display 128 bytes  
starting from 1373:200

D IF0 → Display 128 bytes  
starting from DS:IF0

D 200 300 → Display 128 bytes  
starting from DS:200 to  
DS:300

D CS:200 212 → Display 128  
bytes starting from CS:200  
to CS:212

**[3] ENTER Command (E)**

insert data 1 byte

E ADDRESS [LIST]

Default → DS

E DS:100 FF FF FFFF

عشانه اثنون الي بعدنا (space)   
 و الي قبلنا (dash)

انتيه انحصارونه FFFF   
 [ايضا على سواله]   
 FF0FF في كذا space

\* لوعلى ENTER , ASCII بيظن و ارقام بل Hex   
 "A" → 41

**[4] FILL Command (F)**

⇒ insert blocks of data

F starting address    Ending address    Address List    huge no. of locations

Default → DS

$$\# \text{ of locations} = (\text{ending address} - \text{starting address}) + 1$$

\* لوطيطي   
 1F 55 21 33   
 Locations

**[5] Move Command (M)**

⇒ blocks of 1 copy the data from one part of memory to another

M starting address    END address    DEST Address   
 بداية الجزء الي بيدي   
 انا على   
 بي انصاري

Default → DS

**[6] Compare Command (C)**

⇒ ...

C starting address    end address    DEST address

Default → DS

[7] search command (S)

يتم عن data سيرة

S starting address      end address      Address list  
 address                      address                      list  
 ↓                                      ↓  
 اللى بيدي                      اللى بيدي  
~~اللى بيدي~~                      Search

[8] INPUT Command (I)

1 ADDRESS

لغيرين شرطه " " Address

[9] output command (O)

1 ADDRESS BYTE

data insert

input → Read  
 output → Write

[10] Hexadecimal Command (H)

H NUM 1      NUM 2

NUM1-NUM2  
 ADD

NUM1-NUM2  
 SUB

اللى بيدي ← H 0 □      \* لو بيدي احسن " " 2's  
 = Complement

اللى بيدي ← H physical shifted offset  
 address                      base                      address

11) UNAssemble command (U)

U [starting address] [ending address]

⇒ Convert from machine code to assembly code

Default CS

12) Assemble command (A)

A [starting Address]

⇒ Convert from Assembly language to machine code.

Default CS:100

13) TRACE command (T)

T [starting Address] [NUMBER]

⇒ execute few # of instructions

↓  
رقم  
↓  
تعداد

Default CS:IP

14) Go Command

G [= starting Address] [break point address] [Address list]

↳ will execute the

program

↳ تا زمانی که MAX و بعد از آن

[10]

Default CS:IP

# 5.1 : Data-transfer instructions (flags) (نقل البيانات) CH5

## 1] Move instruction

Mnemonic	Meaning	Format	Operation	Flag affected
MOV	move	MOV, Dis	(S) → (D)	<u>NONE</u>

Source (S) is data  
Destination (D)

Mem → Mem in MOV \* ما ينقل نقل  
seg, const in MOV \* ما ينقل نقل  
البيانات

\* Not-Allowed instructions  
المحظوظة  
تتأثر

بالتسوية Reg ~~البيانات~~ البيانات

Default DS  
عنا في memory  
إذا احتجت

## 2] Exchange instruction

Mnemonic	Meaning	Format	Operation	Flag affected
XCHG	Exchange	XCHG, Dis	(D) ↔ (S)	<u>NONE</u>

D → S  
Source إلى Dest \*  
Dest إلى Source  
S → D

يبدلين

Default DS  
Address من memory  
! memory

\* Not allowed instructions  
const in source  
+ في source

## 3] Translate instruction

Mnemonic	Meaning	Format	Operation	Flags
XLAT	Translate	XLAT	(AL) + (BX) + (DS) → AL	none

جدول الذاكرة EBCDIC  
والبيانات Table في الذاكرة  
memory

ASCI في الذاكرة  
offset to the first element in the table ← BX

البيانات في الذاكرة  
New value for AL  
تكون الذاكرة

AL + BX + DS =  
address التي يتطلع  
في الذاكرة

4

#### 4) Load effective address & load full pointer instructions

Mnemonic	Meaning	Format	Flags affected
LEA	Load effective address	LEA Reg16, EA	None
LDS	Load Register & DS	LDS Reg16, Mem32	None
LES	Load Register & ES	LES Reg16, Mem32	None

#### 1) LEA

LEA Reg16, EA

EA = Reg 11 address \*

LEA Bx, [1234]

Bx = 1234

#### 2) LDS

LDS Reg16, Mem32

First 16 bits → Reg16

Second 16 bits → DS

LDS Bx, 12345678H

Bx = 1234H

DS = 5678H

#### 3) LES

LES Reg16, Mem32

First 16 bits → Reg16

Sec 16 bits → ES

Default	DS
memory // address	ES

\* Advantage → we can load full pointer

~~→~~



## 5.2 1- Arithmetic instructions

### □ Addition instruction

- ADD

Mnemonic	Meaning	Format	Operation	Flags effected
ADD	Addition	ADD D, S	(D) + (S) → D	CF, SF, PF, ZF, OF, AF (RPL)

• رصيد ←

- ADD With Carry

Mnemonic	Meaning	Format	Operation	Flags effected
ADC	Add with Carry	ADC D, S	(D) + (S) + (CF) → Dest	CF, SF, PF, ZF, AF OF

CF → رصيد instruction قبل

OF

- Increment

Mnemonic	Meaning	Format	Operation	Flags effected
INC	increment	INC D	(D) + 1 → Dest	CF, ZF, PF, SF, AF OF X رصيد ←

- ASCII adjust for addition.

Mnemonic	Meaning	Format	Flags effect
AAA	ASCII adjust for addition	AAA	CF, AF → only رصيد ←

Result // رصيد ←  
 AX, AX size // رصيد ←  
 ASCII // رصيد ←  
 AAA // رصيد ←

- Decimal Adjust for addition - DAA

Result // رصيد ←  
 AH, AL // رصيد ←  
 Dec // رصيد ←  
 DAA // رصيد ←

□

# 5-2 - subtraction instructions

Mnemonic	Meaning	Format	Operation	Flags effected
SUB	subtraction	SUB D, S	$(D) - (S) \rightarrow D$	CF, ZF, PF, OF, AF, SF
SBB	subtract with borrow	SBB D, S	$(D) - (S) - CF \rightarrow D$	CF
DEC	Decrement by 1	DEC D	$(D) - 1 \rightarrow D$	CF, ZF, PF, OF, AF, SF
NEG	Negate	NEG D	$0 - D \rightarrow D$ $1 \rightarrow CF$ 2's complement	CF, ZF, PF, OF, AF, SF
AAS	ASCII adjust for SUB	AAS		CF, AF
DAS	Decimal adjust for SUB	DAS		CF, ZF, PF, OF, AF, SF

Addition

3] Multiplication → مطلوب اعرف انه بغيروا لا flags

1] MUL  
↳ unsigned multiply

MUL ≤

AL \* 8 → AX

AX \* 16 → DX AX

بختار AL / AX  
حسب size  
⑤

بهاد العزب مايتخلع على الاشارة وبتكون عزب عادي (استخدم التالوليت اسهل)

2] IMUL  
↳ signed multiply

IMULS

AL \* 8 → AX

AX \* 16 → DX AX

بختار AL / AX  
حسب size source

← تكون لازم اتب على signed حسب MSB  
+ve ← 0  
-ve ← 1  
2's complement

بجرب | وبعدها مرجع باحسب جوابه  
2's complement #  
بعد ما اخوله -ve  
اذا القين -ve  
اذا القين +ve

AX = final Result

اذا كانه واحد  
ب -ve

Result  
AX

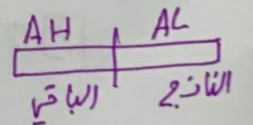
4] Division → مطلوب اعرف انه بغيروا لا flags

1] DIV  
↳ unsigned

DIUS

AX / 8 →

DX AX / 16 →



AX → الناتج  
DX → الباقيا

← الباقي = AX - (الناتج \* 8)

← الباقي = DX AX - (الناتج \* 16) وعشانه تعرف الباقي (الناتج \* 16) = DX AX

2] IDIV  
↳ signed

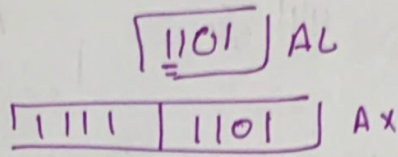
بشوف شو الاشارة حسب MSB  
+ve ← 0  
-ve ← 1  
2's complement

اذا واحد بين -ve الجواب بعد القصة باضه 2's

اذا واحد بين +ve الجواب باضه 2's

\* CBW (convert byte to word)

لے بشرفا // USB لے AL و ربطہ سے آتے ہیں



\* CWD (convert word to double word)

لے بشرفا // USB لے AX و ربطہ سے آتے ہیں

AX = 00110001  
DX = 00000000

5.3 Logic instructions →

علم نظیرا (Logic) اور NOT

1] AND

AND D, S      D.S → D

~~X AND~~

0	0	0
0	1	0
1	0	0
1	1	1

[ X . 1 → no change  
X . 0 → Reset (0)  
میسر ]

2] OR

OR D, S      (D) + (S) → (D)

0	0	0
0	1	1
1	0	1
1	1	1

[ X + 1 → 1 set  
X + 0 → no change ]

3] NOT

NOT D      (D) → D  
0 ↔ 1

4] XOR

XOR D, S      D ⊕ S

0	0	0
0	1	1
1	0	1
1	1	0

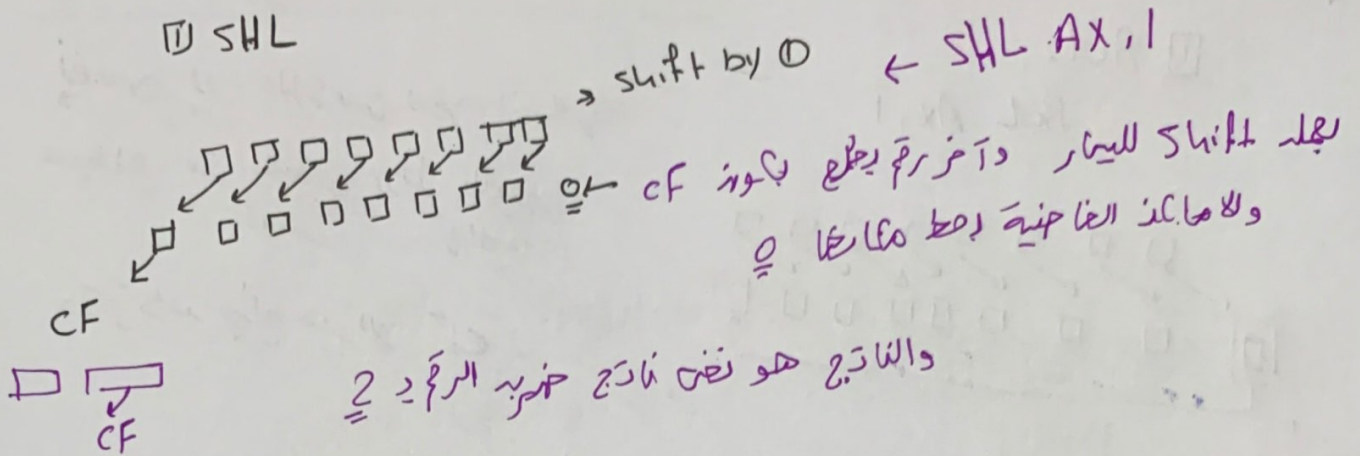
المثابہ ہے 0  
المختلف ہے 1  
ones → even  
↳ 0

ones odd → 1

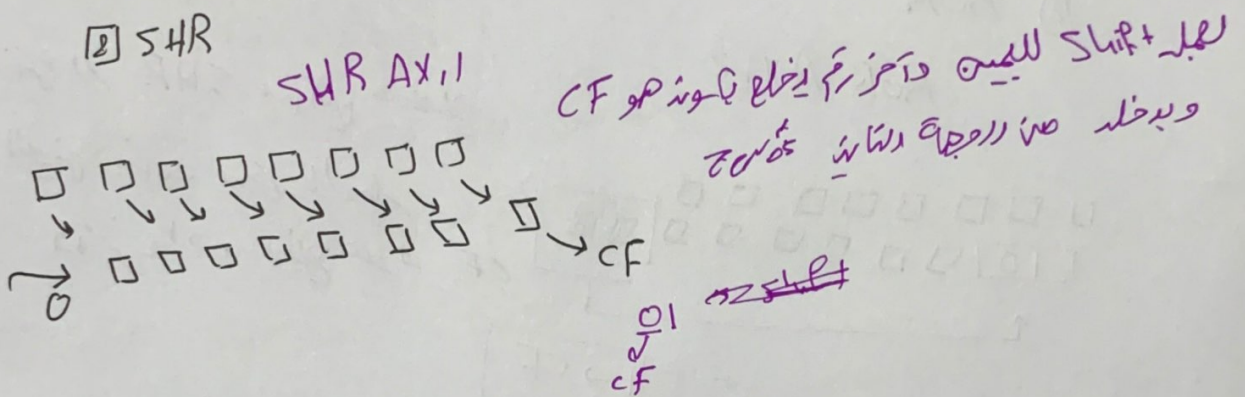
19

5-4 shift instructions ⇒ يعني الحرف انه ال flags بتغيروا

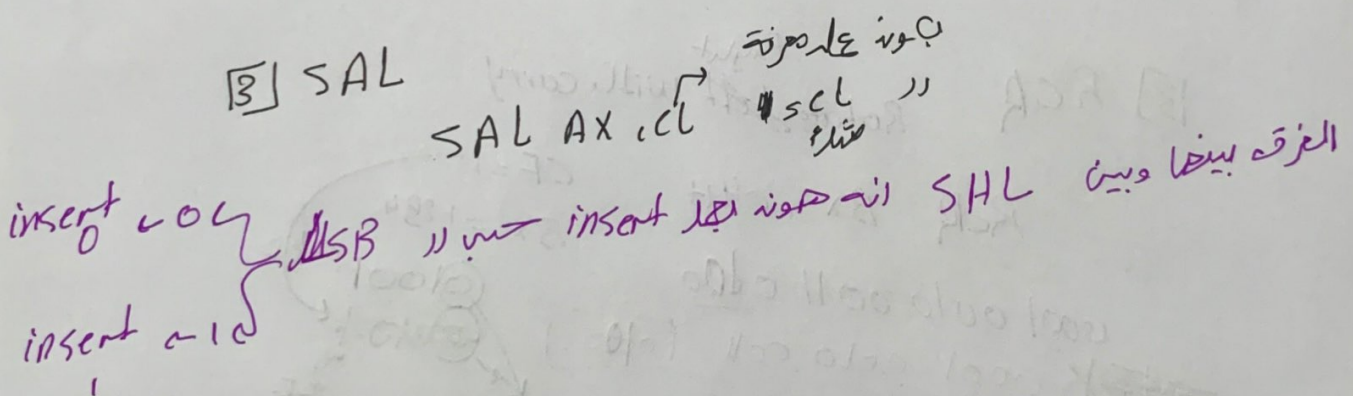
1) SHL



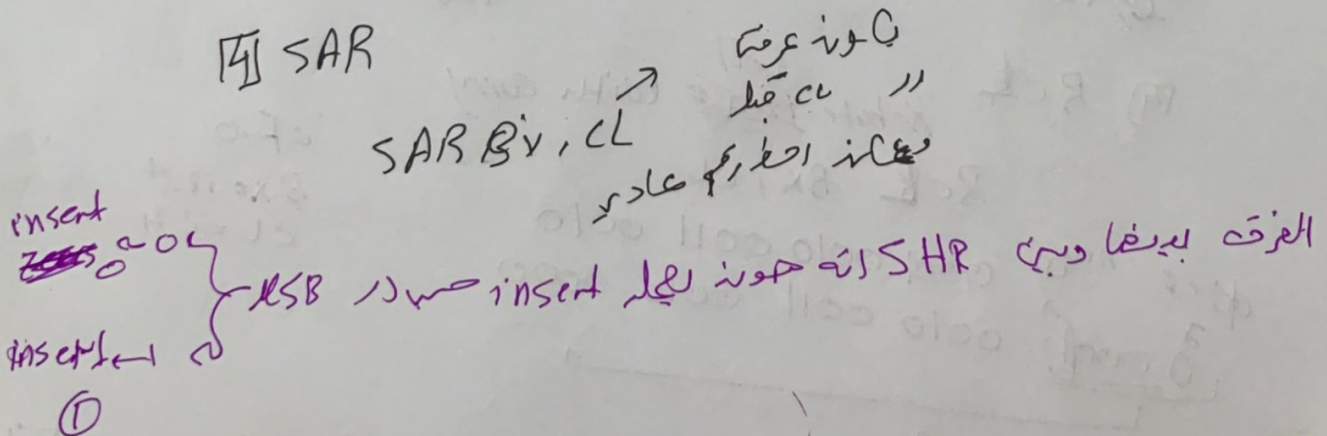
2) SHR



3) SAL



4) SAR

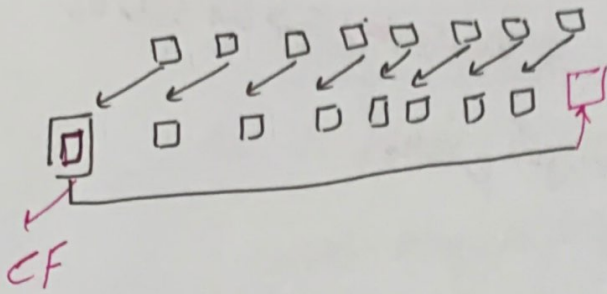


# 5.5 Rotate instructions ⇒

تغيير CF

1) ROL  
ROL AX, 1

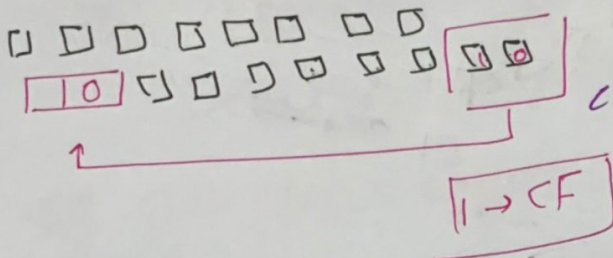
نقلنا من اليمين الى اليسار  
حيث اننا نغيرنا  
البيانات



والاخر واحد يتطلع هو CF

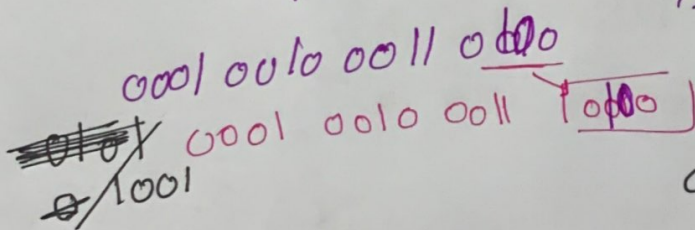
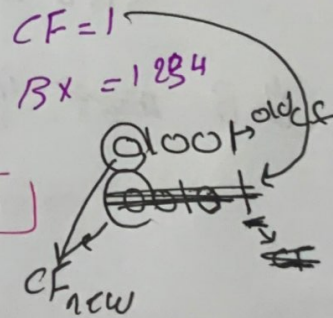
2) ROR  
ROR AX, 2

\* نقلنا من اليمين الى اليسار  
من اليمين نقلنا بيته باليسار  
والاخر واحد يتطلع هو CF



3) RCR  
Rotate ~~Left~~ Right with carry

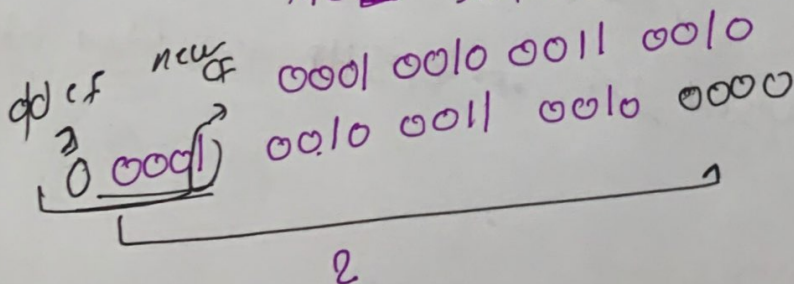
RCR BX, 04H



4) RCL  
Rotate ~~Right~~ Left with carry

RCL BX, CL

CF = 0  
BX = 1234  
CL = 04

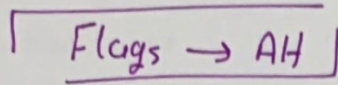


# CH6

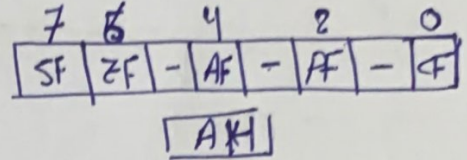
## 6.1 Flag - Control instructions

هدوله از instructions بتغيره بال Flags بطريقة مباشرة

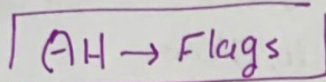
1 Load AH from Flags (LAHF)



بيخذه من الFlags ويضعه بال AH  
له يعني قيمه الFlags ما بتغير



2 STORE AH into flags (SAHF)



بيأخذه من AH ويضعه بال Flags  
له يعني قيمه الFlags بتغير

3 ~~clear~~ clear carry (CLC)

CF = 0

4 Set carry (STC)

CF = 1

5 Complement carry (CMC)

CF = CF̄

\* CLC followed CMC → STC

\* STC followed CMC → CLC

6 clear Interrupt (CLI)

IF = 0

7 set Interrupt (STI)

IF = 1

8 clear direction (CLD)

DF = 0

9 set Direction (STD)

DF = 1

10 → ...

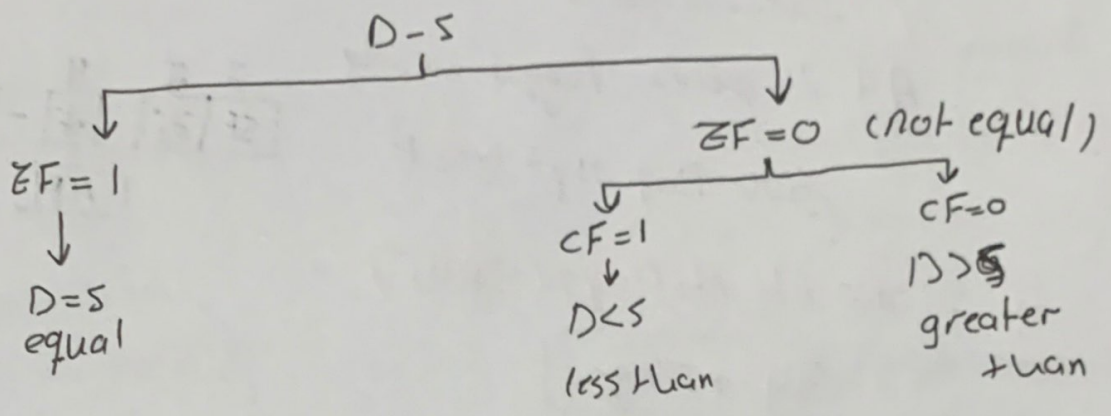
# 6-2 Compare Instruction

CMP D,S

(D) < (S)

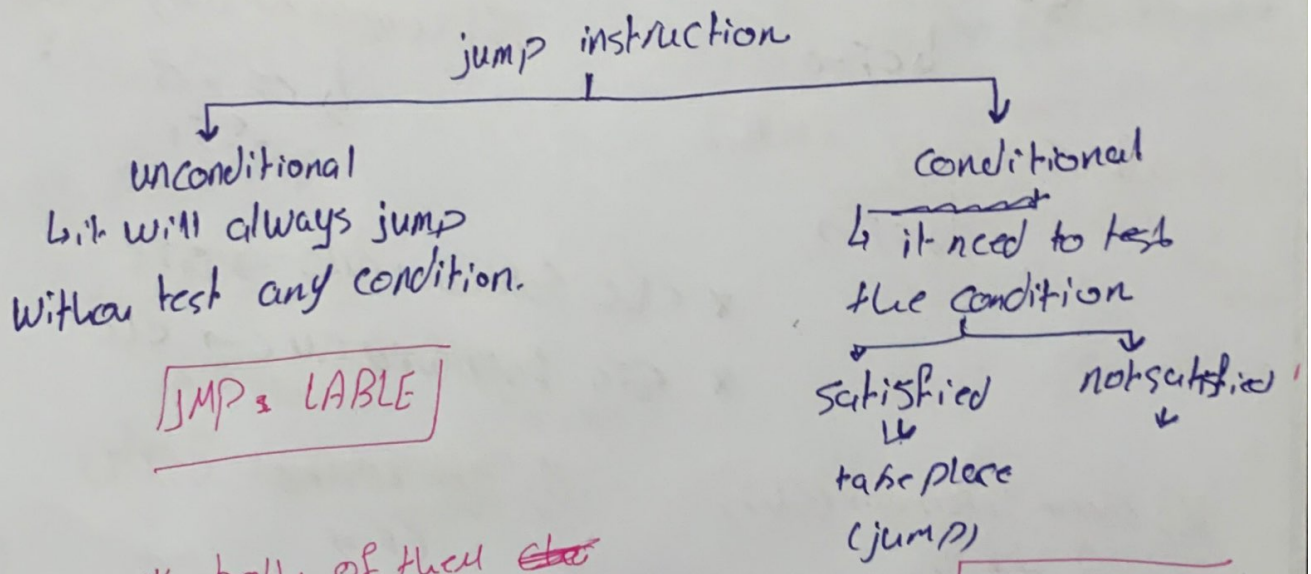
all flags will be effected

ZF, CF, PF, SF, AF, OF



# 6.3 Control flow & jump instruction

↳ change the flow of instruction



```
JMP LABEL
```

```
JCC LABEL
```

\* both of them  
↳ change IP in the same segment

program / LABEL is in IP, & \*  
else jump to is



# JMP/JCC LABEL

Intrasegment Jump

↳ within the same code segment  
(change IP only)

↳ [1] short label  
(label written by 8-bits)

$$IP_{new} = IP_{old} + 8\text{-bits}$$

↳ [2] near label

(size  $\Rightarrow$  16 bits)

$$IP_{new} = \text{near label}$$

↳ [3] Reg ptr 16

$$IP_{new} = \text{value of the Register}$$

\*  $IP_{new} = \text{label} \times Bx$   
for ex  $\text{label} = 100$  (Bx=100)

↳ [4] Mux ptr 16

$IP_{new} \rightarrow$  physical address

$IP_{new}$  is data in bytes

Intersegment Jump

↳ to another code segment  
(change IP & CS)

↳ [1] Far label (inter segment)

32-bits immediate

0-16 bits  $\rightarrow IP_{new}$

17-32 bits  $\rightarrow CS_{new}$

↳ [2] Mux ptr 32 (intersegment)

Mux ptr 16

JMP DWORD PTR [DI]

$DI \cdot DI+1 \rightarrow IP_{new}$

$DI+2 \cdot DI+3 \rightarrow CS_{new}$

في C++ ، if-then-else هي الطريقة  
 للكتابة في Assembly Code باستخدام JMP

C++  
 if  
 ==  
 else  
 ==

في Assembly Code يتم استخدام  
 رج أحلك مثالاً واشرته عتانه تنفيذي الفكرة

	CMP AX, BX	→	اختلاف القيمة (أو لا) (CMP)
if	JE First	→	إذا كانوا equal حينه على First
A == B	JMP END	→	عتانه يطلع من ال (CMP)
B++	JNZ second	→	في حالة ما كانوا (أو لا) مختلفين
else	JMP END	→	ديوجه لهونه بعدين يروح second
B -	second: Dec BX	→	لازم تكونه معرّفها else
	First: Inc BX	→	لازم تكونه معرّفها وحافظة First
	END: ---	→	فيها التي بتي انفره لوجه (if equal)

\* أقرّف تشابه بالعادة  
 احفظ سنواته في جدول

loop program structure

□ Repeat until structure

عدد التكرار → CL

دورة تكرار loop تتكرر (مرة)

CL = 0

وطبعا خلال تكرارها ينفذ instructions

التي موجودة فيها بار code

\* (Force) انه ثابت

MOV CL, Count

Again: ---

---

DEC CL

JNZ Again

[8] while do structure.

نفس فكرة Repeat ضي عدد  $cx$  بما الفرق انما Repeat يكون الشرط اخر ضي بالسور (JNZ gain)

هو (do while) الشرط بالاول (JE next) لا تتصل  $cx$  zero بتطلع هذا loop

JZ	→	بطل jump اذا كان zero	JC	→	بطل jump اذا $cf=1$
JNZ	→	بطل jump اذا لا يتاوى zero			
JE	→	بطل jump اذا كان (equal)			

6.4 → ملاحظة لا يوافق

6.5 the loop & the loop - handling

[1] loop : loop while not zero  
 $cx \neq 0 \rightarrow$  loop بروج اعدوا  $cx-1$  دالة مرة

[2] loopE / loopZ → loop while equal  
 $cx \neq 0$  repeat while count not zero

بشرط  $ZF$   $ZF$   $ZF=1$   $cx \neq 0$  اذا بطل loop  
 $ZF \rightarrow$  loopZ / loopE

β) loopNE / loopNZ  $CX \neq 0$  &  $ZF = 0$   
 ↓

نتيجه من Instruction التي قبله  
 loopNE / loopNE

\* كذا من اطراف loop ← cable و cable short cable

\* اذله شيء بشوف شو ال loop المستخدم

و بعد من شوية اذا مت عيّن بعد ال loop  
 اذا لا بطل من ال loop و حد ال loop

### 6.6 string & string-handling instructions.

قبل ال شيء كذا نعرف ال Direction flag (DF)

DF  $\left\{ \begin{array}{l} \rightarrow 0 \rightarrow \text{forward} \downarrow \\ \rightarrow 1 \rightarrow \text{back word} \uparrow \end{array} \right.$

DF=0 ← CLD  
 DF=1 ← STD

II) Move string (MOVS)

MOVB / MOVSW

(DS)0 + SI → (ES)0 + DI

SI = F1 or F2

DI = F1 or F2

(DS:SI) in Data

(ES:DI) ↓

DI > SI في ال direction

IOR 2 → B / W  
 Byte 0 word 2

F → DF 0 → 0 plain ↓  
 1 → 1 plain ↑

2] Compare / scan string (CMPS / SCAS)

CMPSB / CMPSW

DS:SI - ES:DI

DI = DI + 1 OR + 2

(DS)0 + SI - (ES)0 + DI →

SI = SI + 1 OR + 2

ZF *طابق بين المحتوي الصغير على //*

*دناج العز كانه غير*

• scan

SCASB / SCASW

AL OR AX - ES:DI

AX → Word

AL → Byte

AL OR AX - (ES)0 + DI

*طابق بين المحتوي على // flag*

3] load string

LODSB / LODSW

DS:SI → AL OR AX

AX OR AL } <sup>DS:SI</sup> DS:SI

(DS)0 + SI → AL OR AX

SI =  $\begin{cases} +1 & \text{OR} \\ -2 & \end{cases}$  → W/B *طابق بين المحتوي*

4] store string

STOSB / STOSW

ES:DI } AL OR AX *طابق بين*

AL OR AX → ES:DI

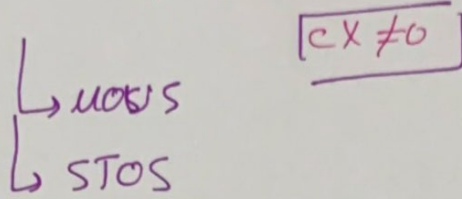
AL OR AX → (ES)0 + DI

DI = DI + 1 OR + 2

# \* Repeat string

REP: Repeat string with the condition  $CX \neq 0$

[1] REP  $\Rightarrow$  Repeat while not end of string



لو اصبحت مع MOV مثلا

ES:DI  $\leftarrow$  DS:SI  $\leftarrow$  MOV S وينقل MOV S

[2]  $CX - 1 = CX$

[3]  $CX \neq 0$  شرط  $CX = 0$  بوقف  
 $CX \neq 0$  شرط

[2] REPE/REPZ  $\Rightarrow CX \neq 0$  ZF = 1  
~~ZF = 0~~  
 { CMPS  
 SCAS

[3] REPNE/REPZ  $CX \neq 0$  ZF = 0  
 { CMPS  
 SCAS

\* فيقول ما هو بالهنا  
 بالهنا